

ABSTRACT OF THE DISCLOSURE

A memory cell that includes a control gate disposed laterally between two floating gates where each floating gate is capable of holding data. Each floating gate in a memory cell may be erased and programmed by applying a combination of voltages to diffusion regions, the control gate, and a well. A plurality of memory cells creates a memory string, and a memory array is formed from a plurality of memory strings arranged in rows and columns.

\* \* \* \* \*